## 4.3 Combined Linear and Δ-Modulated Switched-Mode PA Supply Modulator for Polar Transmitters

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Polar modulation of nonlinear power amplifiers (PAs) is gaining momentum as a method for achieving high-efficiency linear PAs. In polar modulation, the input signal envelope information is typically processed by modulating the PA supply voltage. Wireless broadband linear modulation standards require wide-bandwidth low-distortion high-efficiency supply modulators. Linear low-dropout (LDO) supply modulators have recently been used in polar PAs, as they have low-distortion with a trade-off of poor efficiency at backed-off power [1]. DC-DC switched-mode supply regulators maintain high efficiency over wide output power ranges, but have been used for only narrowband polar PA schemes because of their switching noise and bandwidth limitations [2].

This paper describes a supply modulator that combines a LDO regulator and a switched-mode buck converter. The modulator linearizes a commercial GSM-900 class-C PA using a polar modulation scheme. The presented supply modulator achieves –75dBc noise and harmonic distortion beyond 5MHz bandwidth, and an efficiency of 75.5% at a maximum output power of 30.8dBm. The modulator transmits envelope signals with 20dB voltage dynamic range and 4MHz occupied RF bandwidth.

The supply modulator with the PA load and output envelope feedback is depicted in Fig. 4.3.1. The designed supply modulator is used to modulate the output stage supply voltage of a three-stage saturated class-C PA. The envelope detectors and supply modulator form a feedback loop that is used to monitor the PA output envelope and increase the system linearity. The RF input signal envelope information is processed through the LDO reference voltage input. The LDO supply voltage is varied with respect to the average envelope signal using a Δ-modulated (ΔM) switched-mode buck converter. The switched-mode converter dynamically changes the LDO supply voltage to reduce the I-V drop across the LDO pass device, thus increasing the modulator efficiency over a stand-alone LDO. Because the buck converter regulates frequencies much lower than the envelope signal, the converter maintains high efficiency over a large range of output powers. In stand-alone switched-mode supply modulator topologies, the switching noise directly affects the PA output spectrum, degrading ACPR performance. By combining a switched-mode converter and LDO, the switching noise is attenuated by the power supply rejection (PSR) of the LDO, thus improving ACPR while maintaining efficiency.

The error amplifier of each feedback loop employs a constant $g_m$ rail-to-rail input stage. The LDO error amplifier, shown in Fig. 4.3.2, has a wide swing output buffer as well as active capacitor multiplier Miller-compensation [3]. This enhanced Miller-compensation reduces the feedback capacitors by a factor of 35. The LDO maintains stability for load capacitances between 70pF and 0.1μF. With the PA load, the LDO bandwidth is greater than 4MHz.

The switched-mode buck converter employs a ΔM controller loop, realized with the circuit shown in Fig. 4.3.3 and the switched-mode converter's low-pass output filter (LPF). The error amplifier uses switched-capacitor common-mode feedback. Delta modulation shapes the comparator quantization noise out to higher frequencies with a high-pass response determined by the modulator clocking frequency and LPF bandwidth [2]. For a filter bandwidth of 50kHz and a clock frequency of 10MHz, the highest converter output noise is –48dBc at 300kHz. This noise is passed to the LDO power supply, where it is attenuated by the LDO power supply rejection. The optimum design requires low noise from the switched-mode converter as well as selectively placing the ripple at frequencies with the highest LDO PSR. Since the maximum LDO PSR of –34dB is near 300kHz, a low-pass filter bandwidth of 50kHz gives optimum noise performance at the supply modulator output. To increase effective bandwidth of the switched-mode converter, the converter input signal high frequency content is enhanced by a digital pre-emphasis filter, as shown in Fig. 4.3.1. The digital pre-emphasis filter has an inverse magnitude response of the switched-mode regulator, which compensates the droop caused by the converter LPF from 50kHz to 150kHz.

The supply modulator, envelope detectors, and feedback amplifier are implemented in a 0.25μm CMOS process. All blocks use a 3.3V supply except for the switched-mode converter, which uses a 3.6V supply to allow a maximum LDO output voltage of 2.9V. The supply modulator output power is dynamically adjusted through the LDO reference voltage, and the buck converter output dynamically changes to maintain a constant 0.4V drop across the LDO pass device. Figure 4.3.4 gives a measured performance summary of the supply modulator and shows the measured supply modulator efficiency with respect to the modulator output power. When compared with the measured efficiency of a stand-alone LDO with a constant 3.3V supply, the presented supply modulator shows a 10.6% improvement in efficiency at backed-off powers.

The measured supply modulator output spectrum for a double-sideband (DSB) AM input signal with carrier frequency at 2MHz and tone spacing of 150kHz is shown in Fig. 4.3.5. The switched-mode converter processes a 150kHz input signal to accurately track the average of the envelope signal. The output spectrum is shown for a 50kHz switched-mode converter output filter with digital pre-emphasis, which gives an SNDR over 75dB.

A 1625kb/s data rate, 8PSK linear modulation scheme with 1.8dB peak-to-average power is applied to the amplifier system. For polar modulation, the input signal phase information is upconverted to 900MHz and applied to a commercial GSM-900 PA input, while the envelope information is processed through the LDO. Figure 4.3.6 shows the measured PA output spectrum and $EVM_{rms}$ for the linearized system using the supply modulator compared to a constant supply voltage applied to the commercial PA. The linearized system improves the ACPR by 10dB at a maximum average PA output power of 25.4dBm and RF input frequency of 900MHz. Figure 4.3.7 shows a die micrograph of the supply modulator, envelope detectors, and feedback amplifier with a total chip area of 2.1×2.0mm$^2$.

*Acknowledgements:*
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*References:*
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[2] D. K. Su and W. J. McFarland, "An IC for Linearizing RF Power Amplifiers Using Envelope Elimination and Restoration," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2252-2258, Dec., 1998.
[3] G. A. Rincon-Mora, "Active Capacitor Multiplier in Miller-Compensated Circuits," *IEEE J. Solid-State Circuits*, vol. 35, pp. 26-32, Jan., 2000.

 

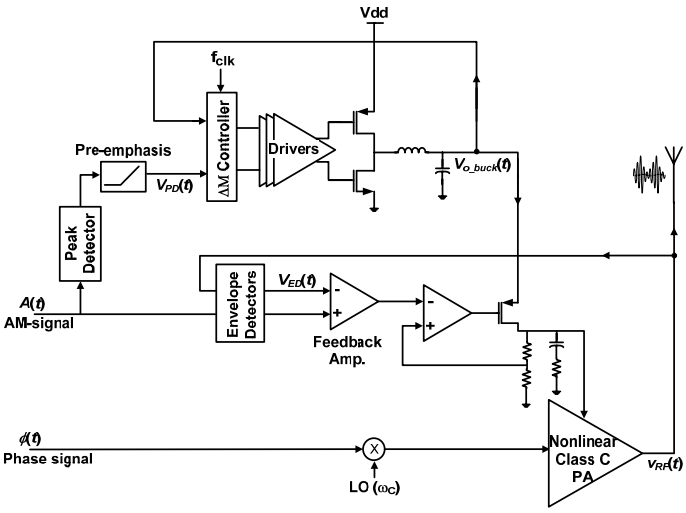


Figure 4.3.1: Supply modulator architecture with PA load.

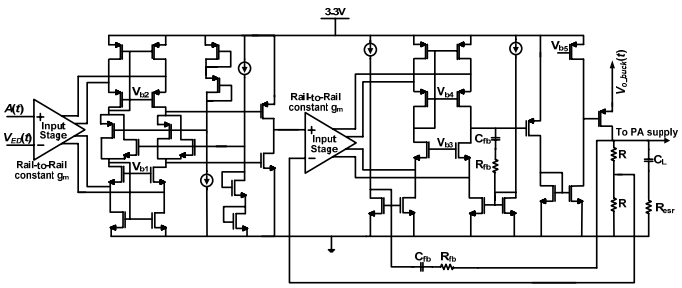


Figure 4.3.2: LDO and feedback amplifier circuits.

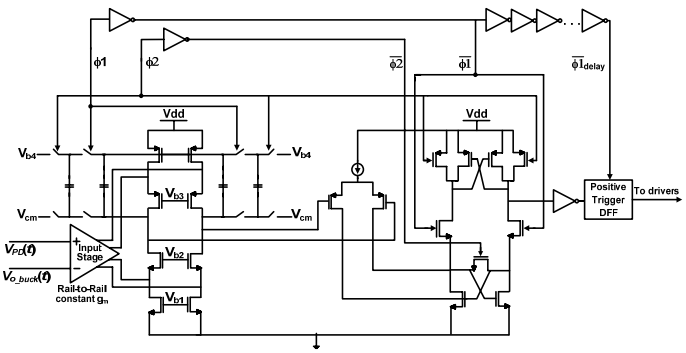


Figure 4.3.3: ΔM control circuit.

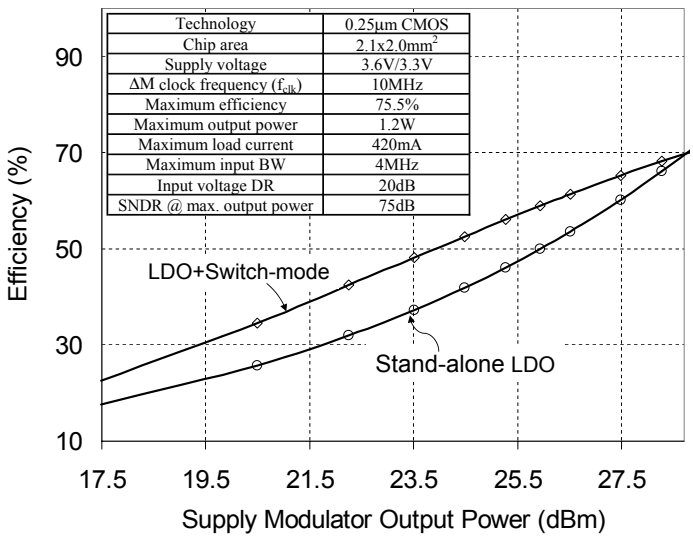


Figure 4.3.4: Measured supply modulator efficiency and performance summary.

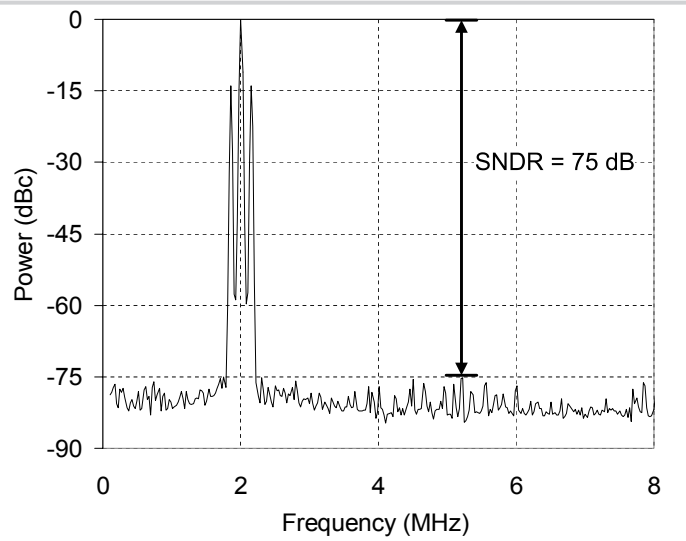


Figure 4.3.5: Measured supply modulator output spectrum for a 2MHz carrier DSB AM input signal.

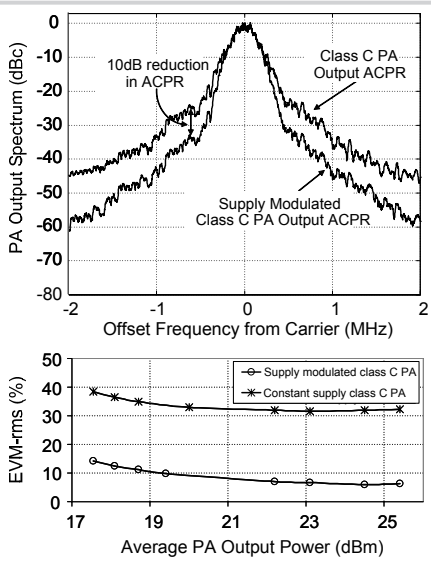


Figure 4.3.6: Measured PA output spectrum and $EVM_{rms}$ for 1625kb/s 8PSK modulation.

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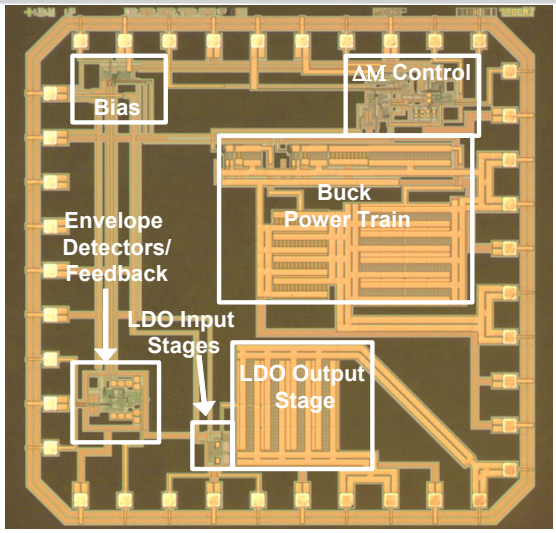


**Figure 4.3.7: Die micrograph of the supply modulator, envelope detectors, and feedback amplifier.**

 